Hall Ticket Number:

Code No. : 13448 S

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) III-Semester Supplementary Examinations, August-2022

Digital System Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Draw the logic diagram of binary to Gray code converter.	2	1	1	1
2.	Show that the dual of the Exclusive-OR is equal to its Complement.	2	2	1	2
3.	Explain the need of carry look ahead adders	2	1	2	2
4.	What are the applications of multiplexer and demultiplexer?	2	1	2	1
5.	Define setup and hold times of Flip Flops.	2	1	3	1
6.	Define state diagram and state table.	2	1	3	2
7.	What are the data types in Verilog HDL?	2	1	4	1
8.	Give the syntax of any two system tasks in Verilog HDL.	2	1	4	1
9.	Mention different types of conditional statements used in Verilog HDL.	2	2	5	1
10.	What is meant by logic synthesis?	2	1	5	1
	Part-B (5×8 = 40 Marks)				
11. a)	Simplify the Boolean function F (w, x, y, z) = Σ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14) using Karnaugh map method.	4	3	1	2
b)	State and Prove De Morgan's Laws.	4	2	1	2
12. a)	Explain the operation of BCD adder with a neat circuit and example.	6	2	2	3
b)	Draw the circuit of 4-to-2-line priority encoder with its truth table	2	3	2	2
13. a)	Explain the design and circuit to convert D-Flip Flop to JK Flip Flop.	4	3	3	2
b)	Implement the 4-bit asynchronous up counter using JK Flip Flops.	4	4	3	3
14. a)	Write Verilog HDL code for 4x1 multiplexer in gate level modelling.	4	2	4	2
b)	Write a Verilog HDL code of a full adder in data flow modelling and its test bench.	4	2	4	2
15. a)	Write Verilog code for 1101 sequence detector using Moore FSM	6	4	5	3
b)	Explain the differences between tasks and functions.	2	2	5	2
16. a)	Explain Binary Codes in Detail.	4	4	1	3
b)	Design a 1-bit comparator using gates? Explain the Procedure.	4	3	2	3

Contd... 2

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17.	Answer any ***two*** of the following:				
a)	Implement a pseudo–Random Binary Sequence Generator with shift registers	4	3	3	3
b)	Give the syntax for regular assignment delay and implicit continuous assignment delay in Verilog.	4	2	4	2
c)	Differentiate between Blocking and Non-Blocking assignments.	4	2	5	2

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20
ii)	Blooms Taxonomy Level – 2	40
iii)	Blooms Taxonomy Level – 3 & 4	40

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